AMENDMENTS TO THE DRAWINGS

Attached hereto is one (1) sheet of corrected formal drawings that comply with the provisions of 37 C.F.R. § 1.84. The corrected formal drawings incorporate the following drawing changes:

Please submit the attached Fig. 7 to replace the original Figure 7, wherein "P+" at the right-hand side is changed to "N+".

It is respectfully requested that the corrected formal drawings be approved and made a part of the record of the above-identified application.

REMARKS

Applicants thank the Examiner for the thorough consideration given the present application. Claims 1-7 are currently being prosecuted. The Examiner is respectfully requested to reconsider his rejections in view of the amendments and Remarks as set forth below.

Drawings

Applicants are submitting a new Figure 7 to correctly label one region. In particular, the region on the right previously labeled P+ is now being labeled N+. No new matter is believed to be involved.

Office Action Summary

The recent Office Action included the Office Action Summary form PTOL-326, which indicated that the action was final. However, the action did not include markings, such as indicating the claims which are pending. Applicants assume that box 4 should have indicated that claims 1-7 are pending and that box 6 should have indicated that claims 1-7 are rejected. If any additional indications were meant to be included by the Examiner, it is requested that the Examiner so indicate in the next action.

Entry of Amendment

The previous action was a final rejection. However, since the present amendment is being submitted along with the Request for Continued Examination, Applicants submit that the entry of the present amendment is required and full consideration of this amendment is requested.

Rejection under 35 U.S.C. 102

Claim 1 stands rejected under 35 U.S.C. 102(a) as being anticipated by Chang et al., (USP 6,469,560). This rejection is respectfully traversed.

The present invention, as shown in Figure 4, is an ESD protection circuit having a resistor device 41, a capacitor device 42, and a PMOS device 43 including gate electrode 431, first electrode 432, second electrode 433, and a bulk electrode 434. Bulk electrode 434 is interconnected to the first electrode 432, and the first electrode is directly connected to the power supply (Vcc).

This differs from the ESD protective circuit disclosed by Chang et al. where the protective circuit includes a PMOS (P2) connected between node A and node C. Node A is the source/drain region of the PMOS and it is connected at one end to the resistor (R2). The other end of the resistor (R2) is connected to the power source (Vcc). Thus, the additional resistor (R2)

is connected between the source/drain region of the PMOS and the power source. Accordingly, the source/drain region of the PMOS is not directly connected to the power source.

In addition, this resistor (R2) is essential for the circuit of Chang et al. During normal operation, the voltage at node B is equal to Vcc such that the PMOS (P2) is turned "off". On the other hand, during an ESD event, the voltage at node A rises because of the resistor (R2) and the parasitic capacity (Cgd). Because the voltage at node B is equal to 0V (grounded) and the PMOS (P2) is turned "on", the voltage at node C will increase close to that at node A when the protective circuit reaches a stable state. Thus, the PMOS merely functions as a switch to make the gate voltages of the two NMOSs (64 and 66) approximately equal during an ESD event. If the resistor (R2) is not present, both of the voltages at node A and node C will always be at a low level, no matter whether the PMOS is turned "on" or not.

Furthermore, in the embodiment shown in Figure 7 of the present application, there is a parasitic diode in the PMOS. In the Chang et al. device, because the voltage at node A is always higher than that at node C, the parasitic diode is ineffectual.

However, parasitic diode is useful in the present invention. Specifically, the PMOS in Figure 7 is used to connect two different voltages, Vcc2 and the voltage at the

common ESD bus 63 referred to as Vcc1. During normal operation, since Vcc2 is higher than Vcc1, the PMOS is turned "off". During an ESD event, if the ESD current flows into Vcc1, it can be directed to Vcc2 through the parasitic diode when the ESD current flows into Vcc2, the PMOS will be turned "on" and the ESD current will be directed to Vcc1 because the gate voltage of the PMOS is close to OV due to the RC time delay. Since PMOS not only functions as a switch but also conducts the ESD current, to prevent a decrease in the conductive efficiency, the two electrodes should not be connected to any resistors.

Furthermore, the ESD current can be directed to either electrode of the PMOS so the ESD protective circuit can be applied to a multi-power integrated circuit. As shown in Figure 6 of the present application, during an ESD event, if the ESD current flows into Vcc1, it will be directed to the common ESD bus 63 by turning "on" the PMOS 613 and then directed to Vcc2 through parasitic diode 71. On the other hand, if the ESD current flows in Vcc2, it will be directed to Vcc1 through a similar mechanism. However, the ESD protective circuit shown by Chang et al. is not suitable for a multi-power integrated circuit since the PMOS merely functions as a switch.

In response to Applicants previous arguments, the Examiner indicated that the language of claims 1 and 3 allows an interpretation that the connection of the electrode to the

power-supply can either mean directly, or connected through a resistor, connected through a capacitor or connected through a semi-conductor. By way of the present amendment, Applicants have amended claims 1 and 3 in order to specify that this connection is a direct connection. Thus, Applicants submit that this language now overcomes the teachings of Chang et al. In view of this, Applicants submit that claim 1 is not anticipated by Chang et al.

Claim 3 is a separate independent claim, which relates to the multiple power-supply embodiment. This claim describes two ESD protection circuits, each having the elements listed in claim 1 and in particular being described as having the first electrode being directly connected to the power supply. Thus, this claim is allowable for the same reason as recited above. Furthermore, this claim is directed to the multiple power supply, which is not possible using the Chang et al. device as discussed above. Accordingly, Applicants submit that this claim likewise is not anticipated by Chang et al.

Claim 2 depends from claim 1 and claims 4-7 depend from claim 2. In view of their dependency from allowable claims, these claims are likewise considered to be allowable.

Rejection under 35 U.S.C. 103

Claims 3 and 5-7 stand rejected under 35 U.S.C. 103(a) as being obvious over Chang et al. As is discussed above, Chang et al. does not show the direct connection for connecting the first electrode to the power source. Further, Applicants submit that changing this connection to a direct connection would not be obvious since this would cause the device to be nonfunctioning as discussed above. In view of this, Applicants submit that the claims are also not obvious over the Chang et al. reference.

Claims 2 and 4 stand rejected under 35 U.S.C. 103(a) as being obvious over Chang et al. in view of Mentzer (USP 5,535,086). This rejection is likewise traversed.

The Examiner cited the Mentzer reference to show the RC time constant circuit of an ESD protection circuit is constructed with a time constant in microseconds. However, Applicants submit that even if this reference does teach this concept, it still does not aid the Chang et al. reference in overcoming its deficiencies noted above, especially the lack of a direct connection. Accordingly, Applicants submit that the claims define over this combination of references as well.

Conclusion

In view of the above remarks, it is believed that the claims clearly distinguish over the patents relied on by the Examiner, either alone or in combination. In view of this, reconsideration of the rejections and allowance of all the claims are respectfully requested.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert F. Gnuse (Reg. No. 27,295) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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KM/RFG:trb
3626-0219P

Attachment(s): Replacement Figure 7

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